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Dynamic Performance Comparison of Conventional and Interleaved Boost Converters under Partial Shading

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ABSTRACT

Photovoltaic (PV) panels under partial shading experience rapid input voltage changes that disturb maximum power point tracking (MPPT). This study aims to compare the performance of a conventional boost converter (LT3757) and a two-phase non-synchronous interleaved boost converter (LTC3787) for a 100 Wp PV system (nominal input 17.7 V, output 24 V). A dynamic simulation was performed in LTspice with input voltage stepping from 17.7 V to 8.5 V (simulating partial shading) and back, while simultaneously switching the load resistance (5.76 Ω for 100 W, 11.52 Ω for 50 W). Measured parameters include input current ripple, efficiency, undershoot, overshoot, and settling time. Results show that the interleaved converter achieves 14% lower input current ripple during the shading transition (6.54 A vs. 7.74 A), much shorter settling time (648 µs vs. 3386 µs), and keeps the output voltage within the ±2% tolerance band throughout the transient, whereas the conventional converter violates the band. Efficiency is nearly identical for both converters (≈96% at 100 W, ≈95% at 50 W). Mathematical analysis reveals that the higher steady-state ripple of the interleaved converter is due to a ripple cancellation factor of only 0.603 at D=0.284 and the smaller inductors (3.3 µH vs. 6.8 µH). It is concluded that for small-scale off-grid PV systems frequently affected by partial shading, the interleaved converter is recommended because of its superior dynamic performance.

***Keywords**: Boost converter, interleaved boost converter, partial shading, LT3757, LTC3787.*

I. INTRODUCTION

Solar photovoltaic (PV) power is an increasingly expanding source of renewable energy. Nonetheless, its effective implementation encounters difficulties because of variable solar irradiance. Partial shading from clouds, surrounding buildings, or collected dust can decrease a PV system's output power by as much as 70% [1][2][3]. Partial shading results in several peaks in the PV power-voltage (P-V) characteristic curve, making maximum power point tracking (MPPT) algorithms more complex and possibly causing them to get stuck at a local maximum [4]. Additionally, increases in temperature have been demonstrated to notably decrease PV output voltage and efficiency [5]. In the meantime, configuration strategies for modules like series-parallel and honeycomb setups can reduce the effects of partial shading and current mismatch [6].

An essential component of PV systems is the DC-DC converter, linking the PV panel to the load or battery. The boost converter is commonly employed to elevate the PV voltage to a greater, regulated DC bus. However, conventional single-phase boost converters face several issues in partial shading situations: substantial input current ripple leading to oscillations close to the MPP, which impacts MPPT accuracy; slow transient response to abrupt changes in irradiance; and lower efficiency at high duty cycles required for low input voltages [7][8].

To address these limitations, interleaved boost converters (IBCs) have been extensively researched. Connecting several converter phases in parallel with a 180° phase difference effectively doubles the input switching frequency, which decreases input current ripple and allows for smaller passive components [9][10]. Interleaved topologies offer enhanced thermal distribution and greater reliability [2][3]. Additionally, interleaved boost converters have demonstrated the ability to reduce partial shading impacts when paired with sophisticated MPPT algorithms [2][4][10][11]. Interleaved boost converters use two or more [12][13][14]. This can decrease input ripple and enable smaller components; however, it creates a more complex circuit.

Even with these progresses, the current literature still has numerous gaps that drive this research. Primarily, the majority of comparative analyses on boost converters for photovoltaic applications assess performance solely under steady-state conditions with unchanging irradiance [8][9][15]. As a result, the dynamic transient behavior—particularly voltage overshoot, undershoot, and settling time—during sudden changes due to partial shading is

seldom measured. Secondly, studies on interleaved topologies mainly concentrate on synchronous rectification (utilizing MOSFETs as synchronous switches) to attain maximum efficiency [16][17]. Nevertheless, synchronous designs raise the number of components and expenses, rendering them less feasible for small-scale, budget-conscious off-grid systems. Third, current interleaved designs for PV are frequently tested at elevated power levels (>200 W) or within grid-connected systems [3], creating a gap for a thorough comparison at the 100 W scale under varying shading conditions.

This study addresses these gaps by contrasting previous works in three significant ways. Initially, we directly simulate partial shading as a sudden variation in input voltage (from 17.7 V to 8.5 V and back), allowing for quantitative assessment of transient metrics (overshoot, undershoot, settling time) that are infrequently considered. Next, we set up the advanced LTC3787 controller to operate in non-synchronous mode—meaning we turn off its internal synchronous MOSFET drivers and implement external Schottky diodes—to assess if the advantages of interleaving (minimal ripple, quick response) can be maintained at a reduced component expense compared to entirely synchronous designs. Third, we present a straightforward one-to-one comparison between a standard single-phase boost (LT3757) and a two-phase interleaved non-synchronous boost (LTC3787) under the same input variations and load conditions for a 100 W off-grid photovoltaic application.

II. METHODOLOGY

This section presents the systematic design process and simulation methodology adopted in this study. The overall research design consists of four main stages: (1) specification of the PV panel and definition of partial shading scenarios based on literature, (2) design of the conventional boost converter using the LT3757 controller, (3) design of the two-phase interleaved non-synchronous boost converter using the LTC3787 controller, and (4) comparative performance evaluation under both full irradiance and partial shading conditions using LTspice transient simulations. All component values were calculated using standard power electronics formulas and then validated through iterative simulation tuning to ensure stable operation and fair comparison between the two topologies. The following subsections detail each stage, including component selection, parameter calculation, and simulation setup.

A. PV Panel Specification and Shading Scenario

A standard 100 Wp monocrystalline photovoltaic panel was chosen as the benchmark source for this research. According to typical datasheets for 100 Wp panels on the market [1][4], the crucial parameters under standard test conditions (STC: 1000 W/m², 25°C) include:

- Maximal power (P_{mpp}): 100 W
- Voltage at peak power (V_{mp}): 17.7 V (usual range 17–18 V)
- Current at peak power (I_{mp}): 5.65 A
- The converter's nominal input voltage is thus established at 17.7 V, indicating full irradiance conditions.

To replicate a critical partial shading scenario, the input voltage is lowered to 8.5 V. This figure is not random; it is based on the proportional connection between output power and voltage reduction during shading. Studies show that partial shading affecting around 75% of a PV panel's surface can decrease its power output by 71–75% [1]. Assuming a linear decrease in voltage for a cautious estimate, a 50% decrease in power would equate to a voltage drop from 17.7 V to around 8.85 V. The research sets 8.5 V as a feasible minimum, indicating extreme shading where the converter must continue to operate steadily. This method enables the assessment of transient performance (overshoot, undershoot, settling time) during sudden irradiance shifts, marking a significant contribution of this study. Consequently, the two operating points are identified as:

- Standard condition: V_{in} = 17.7 V, P_{out} = 100 W
- Partial shading scenario: V_{in} = 8.5 V, P_{out} = 50 W (adjusted to align with actual panel performance during shading)

B. Converter Specifications

Both converters (conventional and interleaved) are designed to meet the following target specifications:

TABLE 1. CONVERTER SPECIFICATIONS

Parameter	Value
Input voltage (normal)	17.7V
Input voltage (partial shading)	8.5V
Output voltage (V_{out})	24V
Output power (normal)	100W
Output power (shading)	50W
Switching frequency per phase (f_sw)	350kHz

From these specifications, the load resistance for each condition can be calculated using Ohm's law:

$$R_{load} = \frac{(V_{out})^2}{P_{out}} \quad (1)$$

For normal operation, $R_{\text{load}} = 5.76\,\Omega$; for partial shading, $R_{\text{load}} = 11.52\,\Omega$. The required output current is:

$$I_{\text{out}} = \frac{P_{\text{out}}}{V_{\text{out}}} \quad (2)$$

Thus, $I_{\text{out,norm}} = 4.17$ A and $I_{\text{out,shade}} = 2.08$ A. The average input current, assuming an efficiency η, is:

$$I_{\text{in,avg}} = \frac{P_{\text{out}}}{\eta \cdot V_{\text{in}}} \quad (3)$$

With $\eta \approx 0.95$, the input current is approximately 5.94 A under normal conditions and 6.19 A under shading. The output capacitor is selected based on the allowed ripple voltage. A common design rule is:

$$C_{\text{out}} = \frac{I_{\text{out}} \cdot D_{\max}}{\Delta V_{\text{out}} \cdot f_{\text{sw}}} \quad (4)$$

Where $D_{\max}$ is the maximum duty cycle and ΔV_{out} is the peak-to-peak ripple voltage. For this design, a standard value of 100 µF (electrolytic) in parallel with 10 µF (ceramic) is used to minimize equivalent series resistance (ESR).

C. Conventional Boost Converter

The conventional boost converter uses the LT3757 current-mode controller [18]. Key component values are calculated using the equations below.

1. Inductor Selection

For a boost converter operating in continuous conduction mode (ccm), the inductor value is chosen to keep the ripple current within a desired range. The duty cycle equation is:

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \tag{5}$$

The inductor current ripple is set to a fraction k (typically 0.3) of the average input current:

$$\Delta I_L = k \times I_{IN,AVG} \tag{6}$$

The required inductance is then:

$$L = \frac{V_{IN} \cdot D}{\Delta I_L \cdot f_{SW}} \tag{7}$$

Using the nominal values ($V_{in} = 17.7$ V, $I_{in,\,avg} = 6.28$ A, $f_{sw} = 350$ kHz), (5)–(7) yield $L \approx 7.06\,\mu$H. The nearest standard value, 6.8 µH, is selected.

2. Frequency Setting

For 350 kHz, based on the LT3757 datasheet the R_t=36.1 kΩ.

3. Feedback Resistor Divider

The output voltage is set by a resistor divider connected to the FBX pin. The internal reference voltage is $V_{FB} = 1.6$ V. With R_1 From FBX to ground and R_2 From V_{out} To FBX:

$$V_{OUT} = V_{FB}\left(1+\frac{R_2}{R_1}\right) \tag{8}$$

Selecting $R_1 = 10$ kΩ, (9) yields $R_2 = 140$ kΩ.

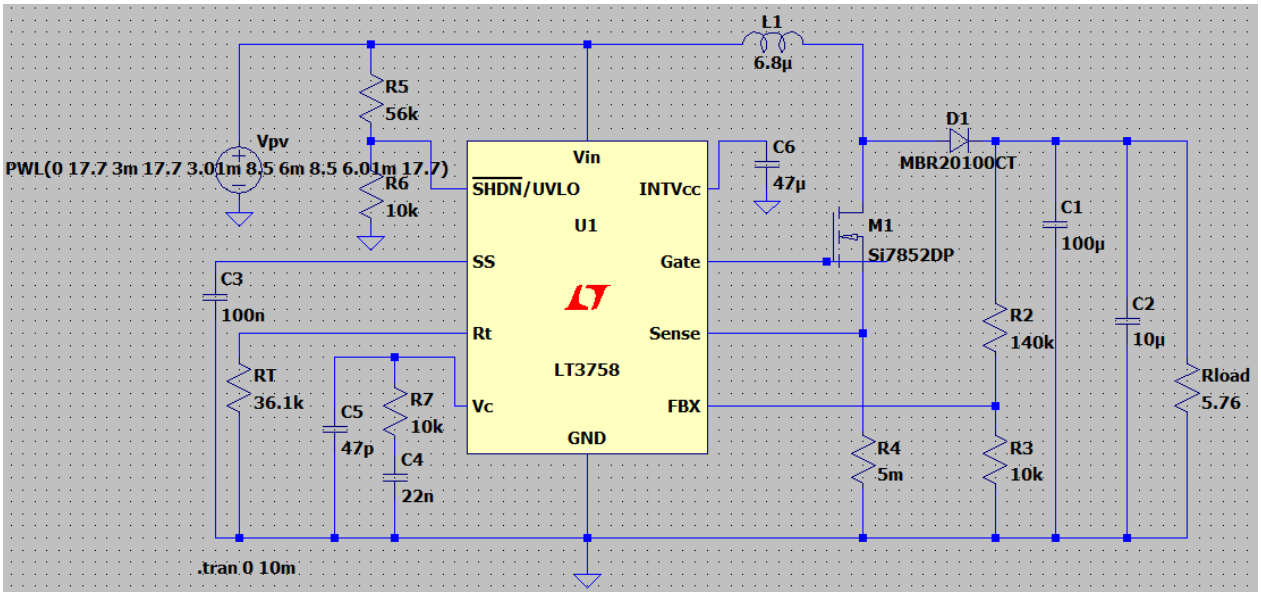

Figure 1. The circuit of the conventional boost converter (LT3757)

TABLE 2. COMPONENTS FOR THE CONVENTIONAL BOOST CONVERTER (LT3757)

Parameter	Specification	Description
Inductor (L)	6.8 µH	Ferrite core, saturation current >4 A
MOSFET (Q)	Si7852DP	N-channel, 30 V, 9.5 A [19]
Diode (D)	MBR20100CT	Schottky, 100 V, 20 A [20]
R_{sense}	5 mΩ	Current sense resistor
R_t (frequency)	36.1 kΩ	Sets f_sw = 350 kHz
R_1 (FB divider)	10 kΩ	Lower resistor
R_2 (FB divider)	140 kΩ	Upper resistor for V_{out} = 24 V
C_{out}	100 Mf + 10 µF	Output filter

D. Interleaved Non-Synchronous Boost Converter

The LTC3787 controller operates in non-synchronous mode with external Schottky diodes in the interleaved converter. The design adheres to the manufacturer's example circuit DC2001A [21].

1. Inductor choice per *Phase*

A standard design guideline suggests setting the inductor ripple at approximately 30% of the average current, necessitating an inductance of roughly 15 µH for each phase. This study, however, utilizes a reduced inductance of 3.3 µH per phase for two reasons. Initially, the DC2001A demonstration board (12 V to 24 V, 240 W, 350 kHz) incorporates 3.3 µH inductors and has demonstrated stability [21]. Secondly, a reduced inductor provides quicker transient response, which is advantageous for PV systems during swift shading alterations. The trade-off involves increased ripple current, but the LTC3787's current-mode control manages it effectively, and the interleaving diminishes the ripple experienced by the PV panel.

2. Feedback divider

The LTC3787 internal voltage reference is 1.2 V. Using (8), with $R_B = 10$ kΩ to ground, we obtain $R_A = 190$ kΩ.

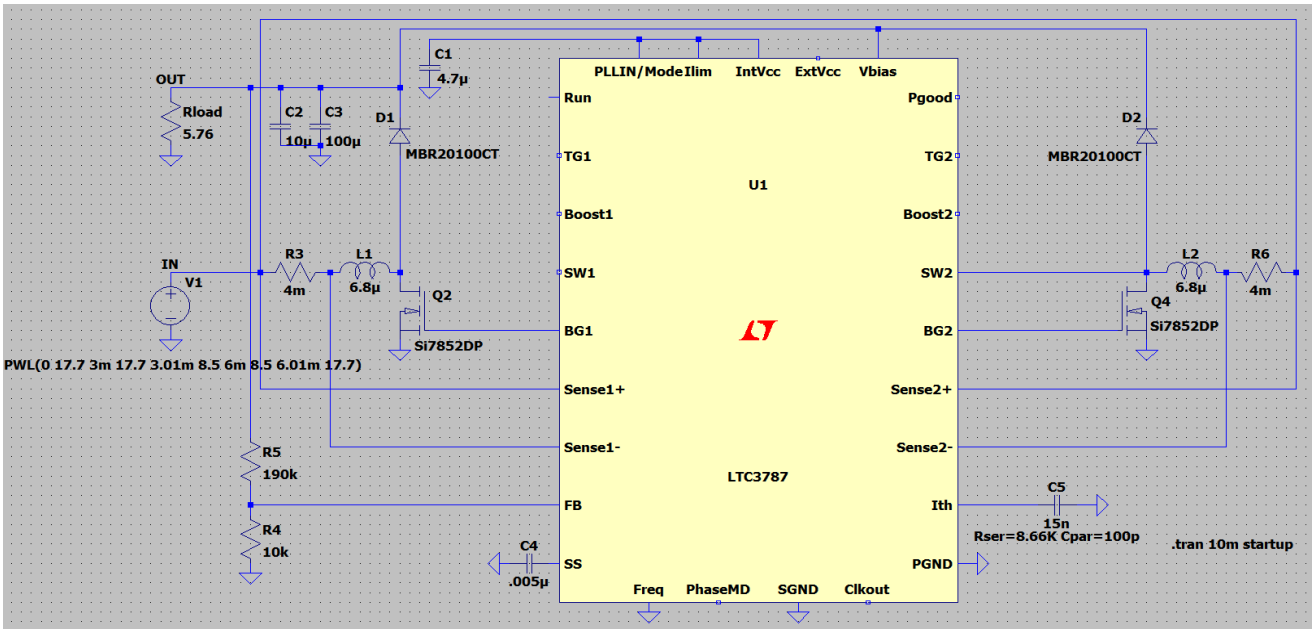

Figure 2. The Circuit of Interleaved non-synchronous boost converter (LTC3787)

TABLE 3. COPONENTS FOR INTERLEAVED NON-SYNCHRONOUS BOOST CONVERTER (LTC3787)

Component	Value	Description
Inductors (L1, L2)	3.3 µH each	Ferrite core, saturation current >8 A
MOSFET (Q)	Si7852DP	N-channel, 30 V, 9.5 A [19]
Diode (D)	MBR20100CT	Schottky, 100 V, 20 A [20]
R_{sense} (each)	5 mΩ	Current sense resistors
R_{FREQ}	Directly to GND	Sets f_sw = 350 kHz per phase
R_B (FB divider low)	10 kΩ	Lower feedback resistor
R_A (FB divider high)	190 kΩ	Upper feedback resistor for 24 V
C_{out}	100 Mf + 10 µF	Output filter

E. Dynamic Simulation Setup

Partial shading was modeled as an ideal step change in the input voltage, as this reflects the most adverse scenario for the converter's transient response. In reality, irradiance changes can occur rapidly (for instance, when the edge of a cloud moves over the panel), and testing with an instantaneous step guarantees that the converter possesses ample dynamic margin. The PWL (Piecewise Linear) source for the input voltage was defined as:

PWL(0 17.7 3m 17.7 3.01m 8.5 6m 8.5 6.01m 17.7)

- 0–3 ms: normal operation (17.7 V, 100 W)
- At 3.01 ms: voltage steps to 8.5 V (shading)
- 3.01–6 ms: shading condition (8.5 V, 50 W)
- At 6.01 ms: voltage steps back to 17.7 V (recovery)
- 6.01–10 ms: normal operation again

To maintain a realistic output power level during shading, the load resistance was changed simultaneously using a second synchronized PWL source:

PWL(0 5.76 3m 5.76 3.01m 11.52 6m 11.52 6.01m 5.76)

Thus, during the shading period (8.5 V input), the output power is reduced to 50 W (since 24 V² / 11.52 Ω = 50 W). The simulation ran for 10 ms with a maximum timestep of 10 ns.

Input current ripple was measured using LTspice .meas PP (peak-to-peak) directives over three time windows:

- 2–2.5 ms: steady-state before shading,
- 2–4 ms: whole period including the shading transition,
- 4–4.5 ms: steady-state after shading.

All components were taken from the LTspice default library. The MOSFET used is Si7852DP [19]; the diode used in both converters is the MBR20100CT Schottky rectifier (20 A, 100 V) [20], which is widely available in the Indonesian market and suitable for photovoltaic applications.

III. RESULTS AND DISCUSSION

A. Verification of Interleaving Operation

We analyze two simulation waveforms to verify that the two phases of the interleaved converter function with a 180° phase shift.

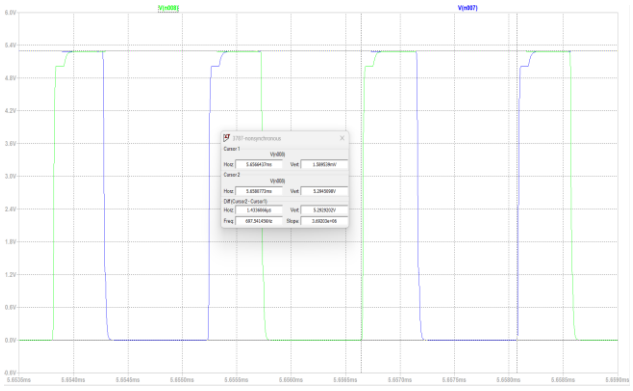

Figure 3. The Gate-drive voltages of the two primary MOSFETs of interleaved boost converter

Initially, the gate-drive voltages of the two primary MOSFETs (T_{G1} and T_{G2}) were graphed. The time interval between the rising edges of T_{G1} and $T_{G2}$was assessed with LTspice cursors. With a switching frequency of 350 kHz, the period is around 2.86 µs. The recorded delay was precisely

1.43 µs, which is half of the period. This verifies that the two phases are displaced by 180°.

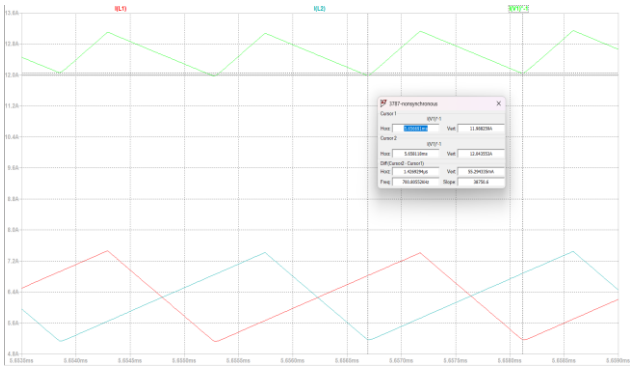

Figure 4. The current inductors of interleaved boost converters

Next, the currents through the inductors I(L_1) and I(L_2) were graphed. The two currents are out of sync: as I(L_1) increases, I(L_2) decreases, and opposite occurs. Consequently, the overall input current (the addition of I(L_1) and I(L_2)) exhibits a ripple frequency of 700 kHz (twice the switching frequency) and a significantly reduced peak-to-peak amplitude. This behavior aligns with the theoretical concept of interleaving. Therefore, the interleaved converter function as expected.

B. Interprettion of Ripple Behavior

The observed behavior can be explained by two physical mechanisms. First, the interleaved converter uses smaller inductors (3.3 µH per phase) than the conventional converter (6.8 µH). During a load step, the current slew rate is governed by di/dt = V/L. The smaller inductors allow a much faster current change, enabling the interleaved topology to respond more quickly to the shading event. Hence, the input current ripple during the transient is significantly reduced.

Second, the theoretical input current ripple cancellation in an interleaved boost converter is most effective when the duty cycle D is near 0.5. At the normal operating point (17.7 V input, 24 V output), $D \approx 0.284$. At this duty cycle, cancellation is incomplete, and the large per-phase ripple of the small inductors can leak into the input. The conventional converter, with its larger inductor, does not rely on cancellation and therefore shows lower steady-state ripple. Table 3 shows the measured peak-to-peak input current ripple.

TABLE 4. INPUT CURRENT RIPPLE (PEAK-TO-PEAK)

Time Window	Conventional (A)	Interleaved (A)	Advantage
2–2.5 ms (normal steady)	2.12	2.62	Conv. better
2–4 ms (including shading)	7.74	6.54	Interleaved better
4–4.5 ms (post-shading steady)	2.34	2.24	Interleaved better

The interleaved converter achieves lower input current ripple during the shading transition (2–4 ms) and also shows lower ripple in the post-shading steady state. Only in the initial steady-state window does the conventional converter have a slight advantage.

C. Efficiency Comparison

Efficiency (η) is calculated using the formula:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\% = \frac{V_{\text{out}} \cdot I_{\text{out}}}{V_{\text{in}} \cdot I_{\text{in}}} \times 100\% \quad (9)$$

where I_{out} is the load current and I_{in} is the average input current. In LTspice, average values are obtained using the .meas command or by visually averaging the steady-state waveform.

In this paper efficiency was calculated directly from the simulation using LTspice's built-in .meas (measure) directives. This approach computes average power over a specified steady-state window, eliminating manual cursor errors and ensuring reproducibility. The following commands were placed in the schematic:

.meas Pin AVG V(in)*I(Vpv) FROM 2m TO 2.5m

.meas Pout AVG V(out)*I(Rload) FROM 2m TO 2.5m

.meas Efficiency PARAM Pout/Pin

Here, V($_{in}$) is the input voltage source (the PV panel model), I(V_{pv}) is the current drawn from it, V(out) is the output voltage, and I(R_{load}) is the current through the load resistor. The time window from 2 ms to 2.5 ms was chosen because both converters reach steady-state well before the first shading event (which occurs at 3.01 ms). This window therefore captures the normal 100 W operating condition without any transient effects. The average power values computed by LTspice are then used to obtain efficiency as:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \quad (10)$$

Table 5 compares the efficiencies of both converters under full irradiance (100 W) and partial shading (50 W) conditions. For the shading condition, a similar .meas window (e.g., 5 ms to 5.5 ms) was used.

TABLE 5. EFFICIENCY COMPARISON

Converter Type	Efficiency (100 W)	Efficiency (50 W)
Conventional (LT3757)	96.36%	94.88%
Interleaved non-sync (LTC3787)	96.28%	94.64%

The interleaved converter attains approximately 0.08–0.24% lower efficiency. The difference is very small and within typical measurement tolerances. For both topologies, efficiency decreases slightly at 50 W because of an increased share of fixed losses (such as gate drive and core losses) relative to the output power.

D. Transient Response to Partial Shading

To assess dynamic performance, the input voltage was stepped from 17.7 V to 8.5 V at t = 3.01 ms (shading) and back at t = 6.01 ms (recovery), with simultaneous load switching.

The output voltage was monitored, and the transient metrics were extracted using LTspice .meas directives. The settling time is defined as the time required for the output

voltage to enter and remain within the ±2% tolerance band (23.52 V–24.48 V) after the step.

TABLE 6. TRANSIENT RESPONSE COMPARISON

Transition	Parameter	Conventional	Interleaved
17.7 V → 8.5 V (shading)	Undershoot	23.02 V (1.18 V below)	23.68 V (0.32 V below)
	Settling time	**3386 µs**	648 µs
8.5 V → 17.7 V (recovery)	Overshoot	25.14 V (1.14 V above)	24.38 V (0.38 V above)
	Settling time	**6309 µs**	198 µs

The interleaved converter exhibits significantly lower undershoot and overshoot. Most importantly, the interleaved converter's undershoot (23.68 V) and overshoot (24.38 V) remain inside the ±2% tolerance band throughout the entire transient. Therefore, its settling time, as measured by the time to first enter the band, is very short (648 µs for shading, 198 µs for recovery). In contrast, the conventional converter violates the tolerance band severely (undershoot to 23.02 V and overshoot to 25.14 V) and requires 3386 µs (3.39 ms) and 6309 µs (6.31 ms) to return to the regulated range.

This superior transient response of the interleaved topology is due to the smaller inductors (3.3 µH per phase vs. 6.8 µH), which allow a much faster current slew rate (di/dt = V/L), enabling the control loop to react more quickly to abrupt changes in input voltage.

E. Discussion

1. Why steady-state ripple is higher for interleaved

At the standard operating point (17.7 V input, 100 W output), the traditional converter shows reduced input current ripple (2.12 A) compared to the interleaved converter (2.62 A). This seems to challenge the widespread belief that interleaving consistently diminishes ripple. Nonetheless, the clarification is found in the duty cycle and the ripple reduction factor.

For a two-phase interleaved boost converter, the ratio of total input ripple to per-phase inductor ripple for $D < 0.5$ is given by:

$$K(D) = \frac{1-2D}{1-D} \tag{11}$$

From the simulation, the duty cycle at normal operation was $D \approx 0.284$. Substituting gives:

$$K(0.284) = \frac{1-0.568}{1-0.284} = \frac{0.432}{0.716} \approx 0.603$$

Thus, the interleaved topology reduces the per-phase ripple to only 60.3% at the input. However, the interleaved converter uses 3.3 µH inductors, while the conventional converter uses 6.8 µH. Since $\Delta I_L \propto 1/L$, the per-phase ripple of the interleaved converter is approximately twice that of the conventional converter. Combining these factors:

$$\Delta I_{in,int} = 0.603 \times (2 \times \Delta I_{L,conv}) = 1.206 \times \Delta I_{L,conv}$$

This theoretical prediction—about 20% higher steady-state ripple for interleaved—matches the simulation results (2.62 A vs. 2.12 A, a 23% difference). Therefore, the behavior is not an error; it is a direct consequence of the chosen inductor values and operating duty cycle. This finding is consistent with the fundamental operating principle of two-phase interleaved converters, where perfect input current ripple cancellation occurs only at exactly 50% duty cycle; at other duty cycles, only partial cancellation is achieved.

2. Superior transient response of the interleaved converter

During the partial shading transition, the interleaved converter exhibits significantly lower input current ripple (6.54 A vs. 7.74 A in the 2–4 ms window) and much better output voltage regulation (undershoot 23.68 V vs. 23.02 V; overshoot 24.38 V vs. 25.14 V). Its settling time is drastically shorter (648 µs vs. 3386 µs for shading; 198 µs vs. 6309 µs for recovery). Moreover, the interleaved converter never violates the ±2% tolerance band, whereas the conventional converter severely exceeds it.

This superior dynamic performance is explained by the smaller inductors (3.3 µH vs. 6.8 µH). The current slew rate is governed by di/dt=V/L; a smaller inductor allows much faster current changes. Consequently, the interleaved topology can rapidly adjust the input current when the load and input voltage change abruptly. This makes it particularly suitable for PV systems that experience rapid irradiance changes due to partial shading.

3. Practical implications for pv system design

Based on the results, the interleaved converter is recommended for PV systems that frequently experience partial shading because:

- It maintains output voltage within regulation limits during shading transients, avoiding over-voltage or under-voltage trips.
- Its settling time is an order of magnitude shorter, ensuring rapid recovery after shading.
- Its efficiency is virtually identical to the conventional converter.

The conventional converter may still be preferred for applications where steady-state ripple is the primary concern and shading is rare. However, for typical off-grid PV installations where shading is common, the dynamic advantages of the interleaved topology outweigh its minor steady-state ripple disadvantage.

4. Limitations of the study and suggestions for future work

We acknowledge several limitations that should be addressed in future research:

- PV panel model: The ideal voltage source used here does not capture the current-limited, non-linear behaviour of real PV panels. Future work should employ a more accurate model (e.g., a current source shunted by a diode and series resistance) to validate the findings under realistic PV characteristics.
- LTC3787 configuration: The LTC3787 is a complex controller with many features (synchronous rectification, phase shedding, etc.). It is possible that

suboptimal settings (e.g., imperfect 180° phase shift, incorrect compensation) contributed to the observed steady-state ripple. A hardware prototype would be necessary to confirm the simulation results.

- Phase-shedding control: At light loads (50 W), the interleaved converter could be operated with only one active phase to reduce fixed losses and improve efficiency. Adaptive phase-shedding algorithms should be investigated.
- Wider operating range: This study examined only two operating points (100 W and 50 W). Future work should sweep over a range of input voltages and load powers to map the duty-cycle regions where each topology is superior.

IV. CONCLUSION

This paper compared a conventional boost converter and a two-phase interleaved non-synchronous boost converter for a 100 Wp PV system under normal and partial shading conditions. A dynamic simulation was performed with simultaneous changes in input voltage and load resistance. Key findings:

1. The interleaved converter achieves 14% lower input current ripple during the shading transition (6.54 A vs. 7.74 A) and maintains output voltage within the ±2% tolerance band throughout the transient, unlike the conventional converter which violates the band severely.
2. Its settling time is drastically shorter (648 µs vs. 3386 µs for shading; 198 µs vs. 6309 µs for recovery).
3. Efficiency is nearly identical (≈96% at 100 W, ≈95% at 50 W), with a negligible advantage for the conventional converter.
4. Mathematical analysis shows that the higher steady-state ripple of the interleaved converter (2.62 A vs. 2.12 A) is a direct consequence of the duty cycle (D≈0.284) and the chosen inductor values (3.3 µH vs. 6.8 µH), not a simulation error.

For low-power off-grid PV systems that frequently experience partial shading, the interleaved converter is recommended because its superior dynamic performance ensures stable output voltage and fast recovery after shading events. Future work should employ a more accurate PV model, verify the LTC3787 configuration experimentally, and explore adaptive phase-shedding control to further improve light-load efficiency.

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